UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,488	09/29/2000	Lester J. Kozlowski	24096.00700	1319

7590 05/17/2004

Doyle B. Johnson
CROSBY, HEAFEY, ROACH & MAY
P O Box 7936
San Francisco, CA 94120-7936

EXAMINER	
MILLER, RYAN J	

ART UNIT	PAPER NUMBER
2621	10

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/675,488	Applicant(s) KOZLOWSKI, LESTER J.	
	Examiner Ryan J. Miller	Art Unit 2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11 and 13-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11 and 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The response received on March 1, 2004 has been placed in the file and was considered by the examiner. An action on the merits follows.

Response to Arguments

2. Applicant's arguments filed March 1, 2004 have been fully considered. A response to these arguments is provided below.

Drawing Objections

Summary of Argument: The applicant argues that the specification has been amended to include the missing reference numerals and that the objections are thereby overcome (see applicant's remarks: page 6, paragraph 1).

Examiner's Response: The examiner agrees. The objection to the drawings has been withdrawn.

37 CFR 1.75 Claim Objections

Summary of Argument: The applicant argues that claim 3 has been cancelled and claim 4 has been amended to overcome the claim objection (see applicant's remarks: page 6, paragraph 2).

Examiner's Response: The examiner agrees. The claim objection has been withdrawn.

Prior Art Rejections

35 U.S.C. 102(e) rejections

Summary of Argument: The applicant argues that independent claims 1, 10, 11, and 14 have been amended to include the tapered reset signal. Therefore, the 35 U.S.C. 102(e) rejections have been overcome (see applicant's remarks: page 6, paragraph 2).

Examiner's Response: The examiner agrees. This limitation is absent from Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1) and, therefore, the reference no longer anticipates the claims. This rejection is withdrawn.

35 U.S.C. 103(a) rejections

Summary of Argument: The applicant argues that a) Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1) has no teaching or suggestion of using a tapered reset signal to reduce the reset noise; instead, Fossum requires two additional means to suppress the reset noise: (1) a photodiode PD and (2) a sample capacitor FD (see applicant's remarks: page 6, paragraph 3). The applicant further argues that b) Kozlowski et al. (U.S. Patent No. 6,439,030 B1) does not teach or suggest low-noise snapshot image formation (see applicant's remarks: page 6, paragraph 4). The applicant also argues that c) combining the circuit of Fossum with Kozlowski et al. to suppress total reset noise is ineffective since FD reset noise is uncorrelated with respect to PD reset noise (see applicant's remarks: page 7, paragraph 1). The applicant finally argues that d) these is no teaching or suggestion in the references to combine them and it is improper to use the applicant's claim as a guide to pick and choose elements or concepts from various references without some teaching or suggestion in the art to make the combination (see applicant's remarks: page 7, paragraph 2).

Examiner's Response: The examiner disagrees. Regarding argument a), the claim does not require that the tapered reset signal is used to reduce the reset noise and, even if the claim did require this feature, it would be regarded merely as an intended use. Therefore, the motivation provided by the examiner in the previous office action is adequate to establish a *prima facie* case of obviousness.

Regarding argument b), none of the claims call for low-noise snapshot image formation. The claims merely call for active pixel sensor circuits comprising a variety of elements.

Regarding argument c), the motivation to combine Fossum and Kozlowski et al. was presented as follows in the previous office action: the use of a tapered reset waveform allows for "a row [to be] resettable to within tens of microseconds for full noise suppression" (see Kozlowski et al.: column 6, lines 51-53). Therefore, the photodiodes of the system can be reset quickly while also suppressing any noise in the signal. Since the claim does not require the suppression of total reset noise, it does not matter that the combination is ineffective at suppressing such noise.

Regarding argument d), in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the use of a tapered reset signal in active pixel sensors has the benefit of allowing "a row [to be] resettable to within tens of microseconds for full noise suppression" (see Kozlowski et al.: column 6, lines 51-53). Therefore, the photodiodes of the system can be reset quickly while also suppressing any noise in the signal. This benefit provides the motivation for using a tapered reset signal in an active pixel sensor system such as the one disclosed in Fossum.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-7, 10, 11, and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1) and Kozlowski et al. (U.S. Patent No. 6,493,030 B1).

As applied to claim 1, Fossum discloses an active pixel sensor circuit comprising: a photodetector (see Fig. 2A: Reference numeral 200); a reset transistor connected between the photodetector and a first bus (see Fig. 2A: Reference numeral 204, referring to transistor M1, which is connected between the photodiode 200 and VDR (i.e. a first bus).); a snapshot transistor having a node connected to the photodetector (see Fig. 2A: Reference numeral 210, referring to transistor M2, which has a node connected to the photodiode 200.) ; a driver transistor connected to a second bus and the snapshot transistor (see Fig. 2A: Reference numeral 216, referring to transistor M4, which is connected to Vdd (i.e. a second bus) and transistor M2 (i.e. the snapshot transistor).); and an isolation transistor connected between the driver transistor and a column bus (see Fig. 2A: Reference numeral 224, referring to transistor M5, which is connected between transistor M4 (i.e. the driver transistor) and column output bus 226.); wherein the transistors are MOSFETs (see paragraph [0022]: The reference describes that transistors are FETs.).

As applied to claim 4, Fossum discloses that a charge from the photodiode is transferred to a gate capacitance of the driver transistor via the snapshot transistor (see paragraph [0031]:

The reference describes that the photosignal (i.e. charge) collected by the photodiode trickles over the TX barrier, which is part of transistor M2 (i.e. a snapshot transistor), to node FD, which is equivalent to the gate capacitance of transistor M4 (i.e. the driver transistor).).

As applied to claim 5, Fossum discloses that the reset transistor discharges any charge left on the photodetector along with any charge on the gate of the driver transistor during a reset operation (see paragraph [0030]: The reference describes that the initial state of the photodiode is erased by the reset operation performed by transistor M1 (i.e. discharges any charge left on the photodetector along with any charge on the gate of the driver transistor during a reset operation).).

As applied to claim 6, Fossum discloses that the reset transistor is disabled during a signal integration mode and a snapshot image capture mode (see Fig. 3C and paragraph [0031]: The reference describes that after the reset, the signal integration and image capture mode are executed. Furthermore, as can be seen in Fig. 3C, no signal is produced for RFD which disables transistor M1 (i.e. the reset transistor).).

As applied to claim 7, Fossum discloses that, after snapshot image capture, the reset transistor is enabled in order to drain any unwanted charge that is generated after the integration mode (see paragraph [0033]: The reference discloses that after the image has been captured, transistor M1 (i.e. the reset transistor) drains all additional photoelectrons form PD down to the level of RFD.).

As applied to claim 10, Fossum discloses an active pixel sensor circuit comprising: photodetector means for converting light into an electrical signal (see Fig. 2A: Reference numeral 200, referring to a photodiode. A photodiode's function is to convert light into an

electrical signal.); image snapshot means connected to the photodetector for transferring the signal from the photodetector (see Fig. 2A and see paragraph [0031]: Reference numeral 210, referring to transistor M2, which is connected to the photodiode 200. This transistor transfers the signal from the photodiode to node FD.); reset means for resetting the photodetector after the image has been transferred (see Fig. 2A and paragraph [0022]: The reference describes a transistor 204 that is used to reset the transistor.); amplifier means for amplifying the signal from the snapshot means (see Fig. 2A and paragraph [0024]: The reference describes that transistor 216 acts as an amplifier.); and isolation means for isolating the circuit from a column bus (see Fig. 2A: Reference numeral 224, referring to transistor M5, which isolates the circuit from column output bus 226.).

As applied to claim 14, Fossum discloses a CMOS imager array comprising a plurality of pixels, each pixel comprising: a photodetector (see Fig. 2A: Reference numeral 200); a reset MOSFET having a source connected to the photodetector, a gate connected to a reset input signal, and a drain connected to a first bus (see Fig. 2A: Reference numeral 204, referring to transistor M1, which has a source connected to the photodiode 200, a gate connected to signal RPD (i.e. a reset input signal), and a drain connected to VDR (i.e. a first bus).); a snapshot MOSFET having a source connected to the photodetector and a gate connected to a snapshot signal (see Fig. 2A: Reference numeral 210, referring to transistor M2, which has a source connected to the photodiode 200 and a gate connected to signal TX (i.e. a snapshot signal).); a driver MOSFET having a drain connected to a second bus and a gate connected to a drain of the snapshot MOSFET (see Fig. 2A: Reference numeral 216, referring to transistor M4, which has a drain connected to Vdd (i.e. a second bus) and a gate connected to a drain of transistor M2 (i.e. a

snapshot MOSFET).); an isolation MOSFET having a drain connected to a source of the driver MOSFET, a gate connected to an access signal, and a source connected to a column bus (see Fig. 2A: Reference numeral 224, referring to transistor M5, which has a drain connected to a source of transistor M4 (i.e. the driver transistor), a gate connected to signal SEL (i.e. an access signal), and a source connected to a column output bus 226.)

As applied to claim 15, Fossum discloses that the reset, snapshot, driver and isolation MOSFETs are all of the same polarity (see Fig. 2A and paragraph [0023]: The reference describes that transistor 210 is an n-well implementation. As can be seen in Fig. 2A, all of the transistors in the schematic are represented by the same symbol. Therefore, all of the transistors have an n-well implementation and are of the same polarity.).

Independent claims 1, 10, and 14 further call for a tapered reset signal to be applied to the reset transistor in order to reset the photodiode. While Fossum discloses the use of a reset signal, RPD, to reset the photodiode, the reference does not disclose that the reset signal is a tapered signal. Kozlowski et al., in the same field of endeavor of active pixel sensors, and the same problem solving area of reset signals, discloses the use of a tapered reset signal (see Fig. 9).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Fossum by adding the tapered reset signal as taught by Kozlowski et al. because the use of a tapered reset waveform allows for "a row [to be] resettable to within tens of microseconds for full noise suppression" (see Kozlowski et al.: column 6, lines 51-53). Therefore, the photodiodes of the system can be reset quickly while also suppressing any noise in the signal.

As applied to claims 11 and 13, which merely call for the method performed by the circuit of claims 1 and 4, since the circuit is disclosed by the combination of Fossum and Kozlowski et al., then the method is also disclosed.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1) and Kozlowski et al. (U.S. Patent No. 6,493,030 B1), as applied to claim 7 above, and further in combination with Uno (U.S. Patent No. 5,296,696 A).

Claim 8 calls for a column buffer to be connected to the column bus. A column buffer is not disclosed by the combination of Fossum and Kozlowski et al. However, Uno, in the same field of endeavor of solid-state image pickup devices discloses the use of such a column buffer (see Fig, 5 and column 4, lines 65-68: The reference describes that an FPN suppression circuit (i.e. a column buffer) is inserted between the column bus and the pixel circuit.).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Fossum and Kozlowski et al. by adding the column buffer as taught in Uno because such a device because such a device suppressed fixed pattern noise while enabling "large output gain and non-destructive readout even with large parasitic capacitances of signal lines" (see Uno: column 3, lines 29-31).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1), Kozlowski et al. (U.S. Patent No. 6,493,030 B1), and Uno (U.S. Patent No. 5,296,696 A), as applied to claim 8 above, and further in combination with Barna et al. (U.S. Patent No. 6,445,022 B1).

Claim 9 calls for a row driver connected to the driver transistor. A row driver is absent from the combination of Fossum, Kozlowski et al., and Uno; however, such a component is disclosed in Barna et al. (see Fig. 5: Reference numeral 508 referring to Row Drivers).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Fossum, Kozlowski et al., and Uno by adding a row driver as disclosed by Barna et al. because the use of a row driver allows the "image array [to be] read out a row at a time" (see Barna et al.: column 3, lines 63-64).

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1) and Kozlowski et al. (U.S. Patent No. 6,493,030 B1), as applied to claim 15 above, and further in combination with Barna et al. (U.S. Patent No. 6,445,022 B1).

Claim 16 calls for a row driver circuit. A row driver circuit is absent from the combination of Fossum and Kozlowski et al.; however Barna et al. discloses the use of such a circuit as described in the rejection of claim 9 above.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Fossum and Kozlowski et al. by adding the row driver circuit disclosed by Barna et al. for the same reasons as described above in the rejection of claim 9.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fossum (U.S. Patent Application Publication No. US 2003/0103153 A1), Kozlowski et al. (U.S. Patent No. 6,493,030 B1), and Barna et al. (U.S. Patent No. 6,445,022 B1), as applied to claim 16 above, and further in combination with Uno (U.S. Patent No. 5,296,696 A).

Claim 17 calls for a column buffer circuit to be connected to the column bus. A column buffer is not disclosed by the combination of Fossum, Kozlowski et al., and Barna et al. However, Uno, in the same field of endeavor of solid-state image pickup devices discloses the use of such a column buffer as described above in the rejection of claim 8.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Fossum, Kozlowski et al., and Barna et al. by adding the column buffer taught in Uno for the same reasons as described above in the rejection of claim 8.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J. Miller whose telephone number is (703) 306-4142. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo H. Boudreau can be reached on (703) 305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan J. Miller
Examiner
Art Unit 2621

Ryan J. Miller

LEO BOUDREAU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600